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Simulation and Performance of Double Gate FinFET Devices

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Abstract
The need for scaling the device is predominant. In this Paper we are scaling the FinFET size, the DIBL Leakage current is decreased and it is calculated. Like normal MOS technology the short channel effect and tunneling effect have been overcome by using High k dielectric material. Here Bottom up approach is followed and the modeling is done by using Silvaco TCAD ATLAS 3D Simulator. The results and problems are briefly discussed.

Keywords
FinFET, Drain Induced Barrier Lowering, Tunneling, Short Channel Effect, Double Gate

I. Introduction

FinFET is the promising device which scales down the size of the device beyond the limit and as well as the performance of the device is not compensated. "The number of transistors per chip would quadruple every three years" this was predicted by Moore decades back and is widely known as Moore's law and has been remarkably followed by Semiconductor industry. [1, 6].

FinFET is designed in 16 nm technology with supporting parameters of width and length. DG FinFET has an excellent scalability and better short channel effect immunity compared to normal MOSFET device. High-k dielectric can be used in DG FinFET [2] [3].While using the high-k dielectric materials, reduces the issues associated with gate leakage and increases the drain current. The DIBL current is calculated. Tunneling can be overcome using high end materials such as TiN [1] [4].Here Bottom up approach is followed to model a FinFET device in Silvaco TCAD. This tool is used to find the performance of the devices. ATLAS 3D Simulator is used for generating 3D diagrams and graphs.

II. Design And Simulation

Mainly focused objectives are:

1. The size of device is scaling down without affecting the performance of the device.
2. The problem is addressed using various technologies, The DIBL current is calculated for using both low k dielectric and High k dielectric materials.

DG FinFETs it consist a Front gate (G1) and an back gate (G2) which provides a better control over Drain Induced Barrier Lowering (DIBL) and Sub threshold slope S. Fin length and other parameters such as length and width is derived from the Poisson's Equation.[5]. The dimensions of the fin determines

The effective channel length and gate width of the device been used. FinFETs comes from the constant fin height constraint the width of the FinFET device can be defined as,

$$W = 2Hfin + Tfin$$

Where Hfin and Tfin are the fin height and thickness respectively. The Modeling is adapted with sequential flow to achieve a complete design: 1) Substrate and High k dielectric material formation 2) Fin Formation 3) Source and drain extension implant 4) Meshing and Region Formation 5) Doping Profiles Implant 5) Electrode Implant [5].

A. Doping Profiles

The doping concentration should be very high for proper device operation. Source and drain both are doped with Phosphorous atom with 1e+20 concentrations and Fin is doped with Boron atom with concentration of 1e+17.

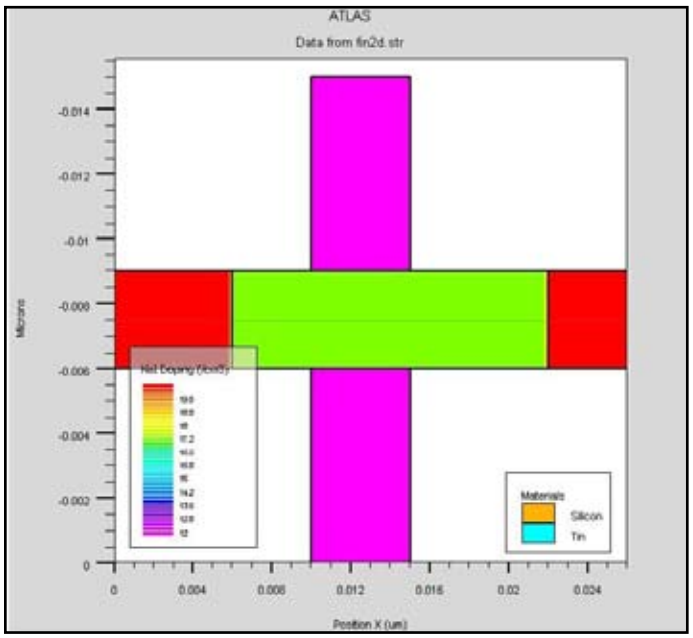

Fig.1: Doping Diagram Of DG FinFET

Here Fig 1 represents the exact doping profiles of Double gate FinFET.

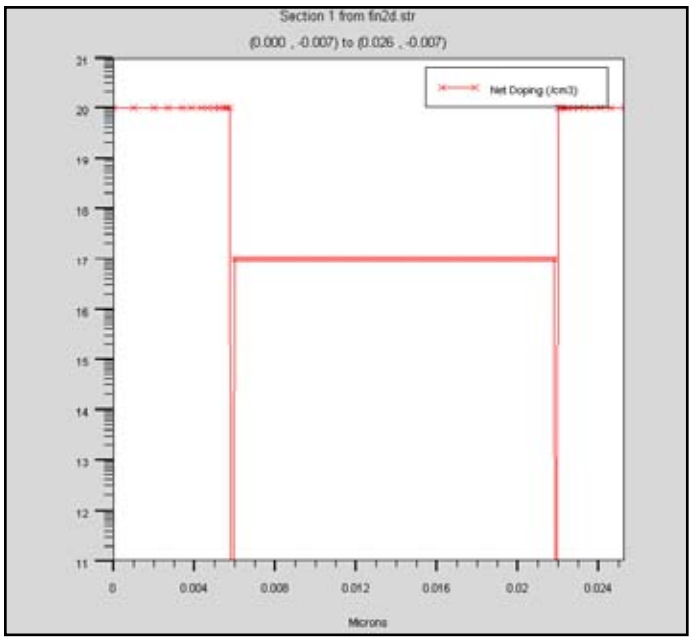

Fig.2: Meshing Lines

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Fig 2 Represents the No.of meshing lines present in the modeling device. For better drain current the number of meshing lines should be more dense.

B. Parameters

All the parameters using in this FinFET is directly derived from Poisson's Equation. If the dimensions are highly scaled then there may be no results. We can't get the expected output and the DIBL Leakage ratio also high. The exact parameters are showed in the table.

Table 1: DG FinFET Parameters

Materials	Length	Doping Concentration	Doping Materials
Source	3 nm	1e20	Phosphorous
Drain	3 nm	1e20	Phosphorous
Fin	16 nm	1e17	Boron
Substrate	22 nm	---	Silicon
Dielectric	22 nm	---	HfO2
Gate 1	4 nm	--	--
Gate 2	4 nm		

C. Complete Design

Here Fig 3 shows the complete modeled design of 16 nm DG FinFET device modeling using Silvaco ATLAS 3D Simulator. All the doping and meshing strategies should be done and Aluminum acts as a conducing material.

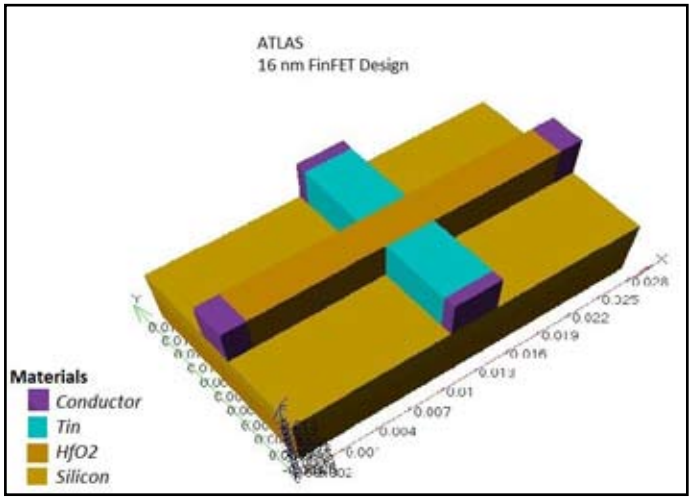

Fig.3: 16 nm DG FinFET

III. Results And Discussons

As the dimensions of transistors are shrunk, the close proximity between the source and the drain reduces the ability of the gate electrode to control the potential distribution and the flow of current in the channel region, and undesirable effects, called the "short-channel effects".[6]

$$I_{\text{leak}} = \sum_{i=1}^{n} C \frac{W}{n} e^{-\frac{qVTi}{mkT}} = \sum_{i=1}^{n} C \frac{W}{n} e^{-BVTi}$$

Where W is the total width of the FinFET device, T is the temperature, m is the body effect coefficient, q is electron charge, k is Boltzmann's constant, and C is a technology parameter. The threshold voltage (V_{Ti},) [8].

Table 2 : DIBL Calculation

Dielectric Used	Gate Oxide Thickness	DIBL (mV)
SiO2	1.3 nm	121
SiO2	2.0 nm	119
SiO2	2.5 nm	117
HfO2	1.3 nm	116
HfO2	2.0 nm	112
HfO2	2.5 nm	110

The FinFET device should be modeled with different gate oxide thickness and the values are be tabulated. And these results are compared with both High k and Low k dielectric materials.

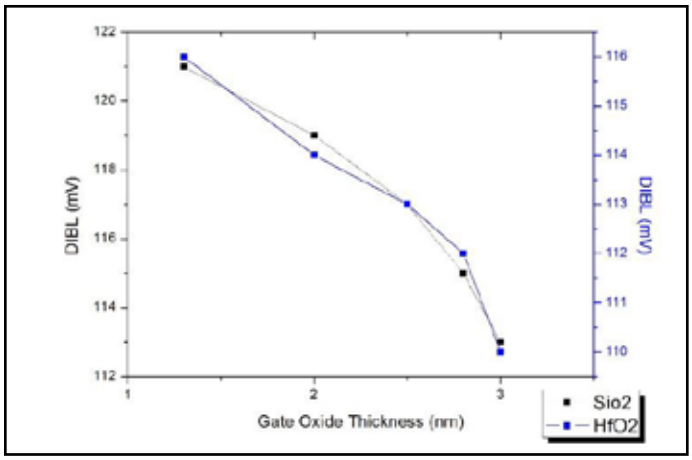

Fig.4 : DIBL Leakage Current SiO2 vs HfO2

When we are using High k dielectric material the leakage current is reduced optimally. In a Multi gate FET the current drive is essentially equal to the sum of the currents flowing along all the interfaces covered by the gate electrode.

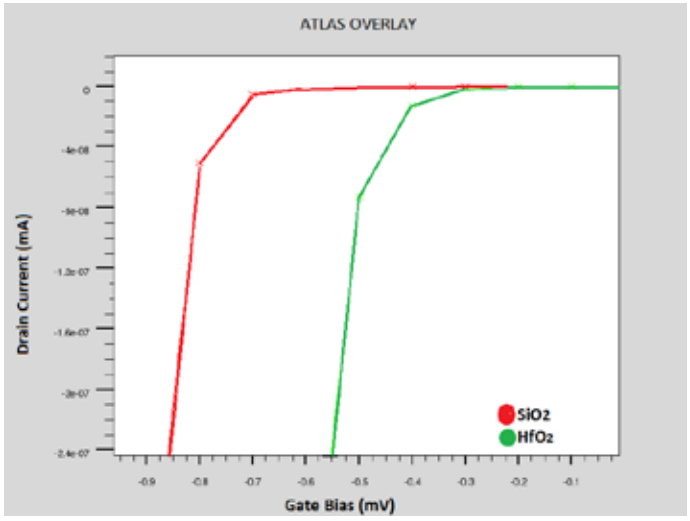

Fig.5: DIBL Leakage current Graph

If a gate Oxide is tightened the electrons in channel may enter into oxide region. This is known as Tunneling. For gate TiN material is used. [2] While using TiN as gate material it will reduce the tunneling current through base and increase the current from source to drain. Because of using independent gates a better

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control in the variation of threshold voltage can be obtained and the dielectric constant value also High.

IV. Conclusions

The Double Gate FinFET device was modeled with the desirable parameters and is tabulated in Table II. Using high k dielectric materials the Short Channel Effects are decreased and DIBL leakage current is calculated. Comparatively results and graphs with 30 nm FinFET the performance of the device is increased, also the leakage current are reduced by 9.51 %.

V. Acknowledgement

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