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Clock Gating: A Comprehensive Power Optimization Technique for Sequential Circuits

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Abstract
Low power is the most critical issues in today's ASIC design, as the feature size is scaled down. Hence there is a urgent need for power optimization. Clock gating is one of the most elegant and classic techniques for reduction of dynamic power, major contributor in total power consumption of any VLSI circuit. Clock gating technique enables saving of electrical power used by computer processors. It ensures power saving by turning on a functional logic block clock, but only when required. Clock gating was the mainstay of the Pentium 4 architecture's power saving modes. This paper presents a review of existing clock gating techniques and its advantages and disadvantages with a demo of D flip flop and 4 bit Pseudo Random Binary Sequence Generator.

Keywords
A*SIC (appplication specific integrated circuits), Clock Gating (CG), latch free clock gating, latch based clock gating, Psuedo Random Binary Sequence Generator (PRBS), Linear feedback shift register (LFSR), Very large scale integration (VLSI).*

I. Introduction

In today's semiconductor designs, lower power consumption is mandatory for mobile and handheld applications for longer battery life and even networking or storage devices for low carbon footprint requirements. Clock power consumes 60-70 percent of total chip power and is expected to significantly increase in the next generation of designs at 45nm and below. This is due to the fact that power is directly proportional to voltage and the frequency of the clock as shown in the following equation:

$$P = CV^2f \quad (1)$$

Hence, reducing clock power is very important. Clock gating is a key power reduction technique used by many designers [1] and is typically implemented by gate-level power synthesis tools.

Clock gating works by efficiently utilizing the clock signals on sequential or synchronous circuits, mostly found in computer processors. Typically, clock gating is implemented in the form of integrated clock gating cells [2]. It manages the clock tree in a way that uses less portions of the circuitry, resulting in reduced flip-flop switching. This leads to power saving that is previously incurred by switching flip flop states. It also leads to less die area, as its replaces muxes with clock gating logic.

This paper discusses the principle of clock gating in section II and demonstrates the various ways to achieve this with design examples of D flip flop and 4-Bit PRBS generator for achieving lower power in section III and also highlight their do's and don'ts to avoid chip failures and unnecessary power dissipation. Conclusions are made in section IV.

II. Clock Gating

Several techniques to reduce the dynamic power have been developed, of which clock gating is predominant. Ordinarily, when a logic unit is clocked, its underlying sequential elements receive the clock signal regardless of whether or not they will toggle in the next cycle.

Clock enabling signals are usually introduced by designers during the system and clock design phases, where the inter-dependencies of the various functions are well understood. In contrast, it is very difficult to define such signals in the gate level, especially in control logic, since the inter-dependencies among the states of various flip-flops depend on automatically synthesized logic. There is a big gap between block disabling that is driven from the HDL definitions, and what can be achieved with data knowledge regarding the flip-flops activities and how they are correlated with each other.

The clock gating technique has been developed to avoid unnecessary power consumptions, like the power wasted by timing components during the time when the system is idle. Specifically for flip-flops, clock gating means disabling the clock signal when the input data does not alter the stored data. It can be applied from the system level where the entire functional unit can be selectively set into sleep mode, or from the sequential/combinational circuit level where some parts of the circuit are in sleep mode while the rest of the block are operating.

But Clock gating does not come for free. Extra logic and interconnects are required to generate the clock enabling signals, and the resulting area and power overhead must be considered [5]. In the extreme case, each clock input of a flip-flop can be disabled individually, yielding maximum clock separation. This, however, results in high overhead. Thus, the clock disabling circuit is shared by a group of several flip-flops in an attempt to reduce the overhead.

(i). How to implement Clock Gating?

When there is no activity at a register "data" input, there is no need to clock the register and hence the "clock" can be gated to switch it off [5]. If the clock feeds a bank of registers, an "enable" signal can be used to gate the clock, which is called the "clock gating enable".

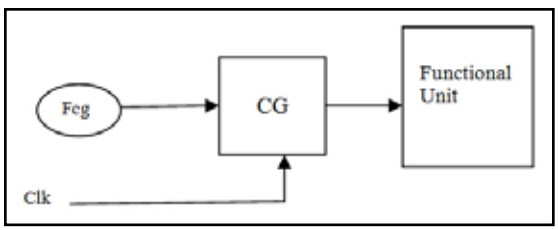

Fig. 1: Clock Gating Principle

The basic principle behind this power optimization technique is as shown in fig.1 [3]. The clock signal is computed by a function

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Fcg, here CLK is the systems clock signal and CLKG is the gated clock of the functional unit. So whenever the clock signal is not needed, unwanted switching activities will be suppressed and hence dynamic power reduces.

III. Available Techniques and Its Demonstration

There are four different optimizing techniques available for clock gating as discussed below

1) Latch-free based design. [1][4]
2) Latch-based design. [1][4]
3) Flip-flop based design. [1][4]
4) Intelligent clock gating optimizing option available in synthesis tool. [1]

(i). Latch-free based design

This is one of the simplest clock gating technique in the design. It makes use of a simple "AND" or "OR" gate for the gating the clock signal in sequential circuit [1]. For sequential circuits operating on negative edge trigger "AND" gate is used, and for the circuits operating on the positive edge of clock "OR" gate is used.

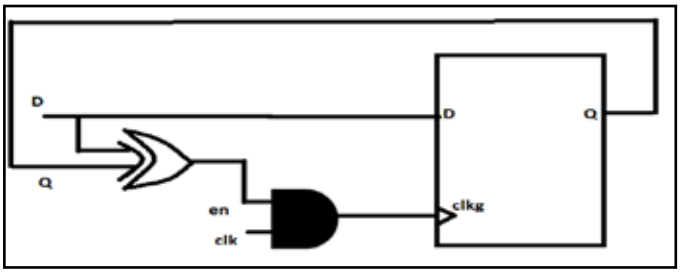

Fig. 2 : Negative edge D flip flop (latch free based design)

These gates (AND or OR) must not alter the waveform of the clock signal, it should just turn on or off the clock signal as per our requirement. This type of clock gating may result in set up or hold time violations. The problem here is if enable signal goes inactive between the clock pulses then gated clock output can terminate prematurely or gated clock signal might get generated of unequal widths [5].

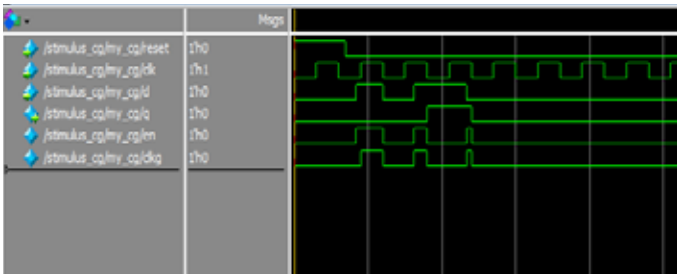

Fig. 3 : Negative edge D flip flop waveform (latch free based design)

Glitches may occur in the gated clock if clock gating is not done properly. For example if the "AND" gate is used for circuits operating on positive edge of clock pulse.The result of this type of clock gating technique on a D flip flop is as shown

Next let's take a 4 bit Pseudo Random Binary Sequence generator example. Pseudo random binary sequence is essentially a random sequence of binary numbers. So PRBS generator is nothing but random binary number generator. The implementation of PRBS generator is based on the linear feedback shift register (LFSR) [6].

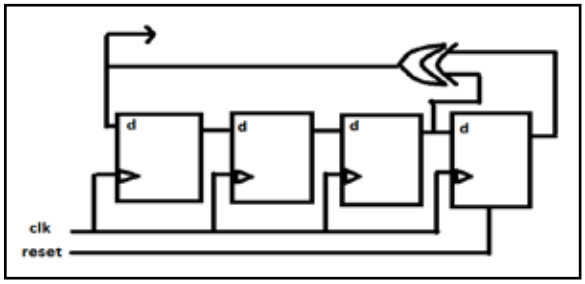

Fig. 4 : A 4-bit Pseudo Random Binary Sequence Generator

Applying a latch free based clock gating technique on this 4-Bit Pseudo Random Binary Sequence Generator, the simulation results are as shown in fig.5.

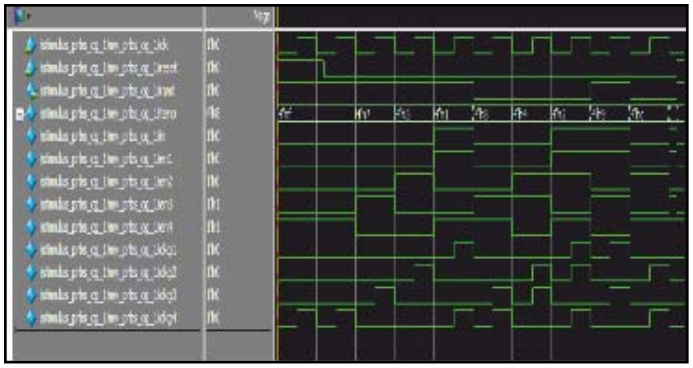

Fig. 5 : 4-bit Pseudo Random Binary Sequence generator (latch free based design)

(ii). Latch based design

In latch based clock gating technique, a level sensitive latch is used as the control element, to control the Enable pin, that is fed to the "AND" or "OR" gate for gating the clock signal. This latch is allowed to reflect the change of Enable pin [1]. The latch holds the value of enable signal from the active edge of the clock till the inactive edge of the clock.

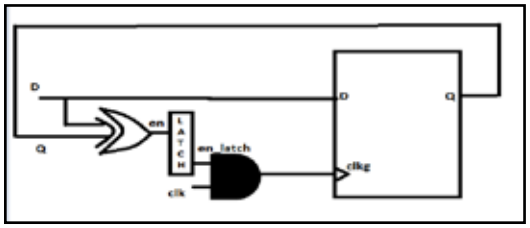

Fig. 6: Negative edge D flip flop (latch based design)

- In this technique no glitch problem arises as in a latch free based design, as latch holds the state of enable till complete pulse is done.
- It's an easy to apply technique.
- However the delay of logic for the computation of enable on the critical path of the circuit will increase thereby effecting the time verification.

The result of this type of clock gating technique on a D flip flop is as shown in fig 7 and for 4-Bit Pseudo Random Binary Sequence Generator simulation results are as shown in fig.8

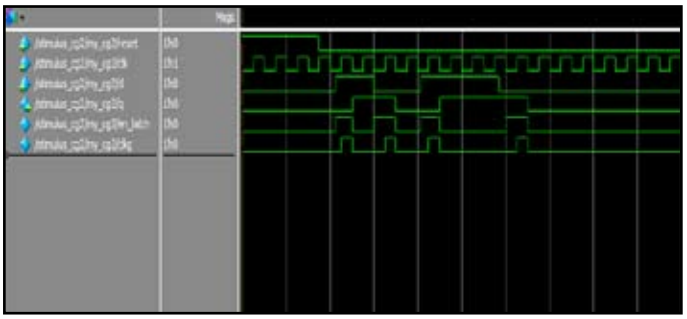

Fig.7 : Negative edge D flip flopwaveform (latch based design)

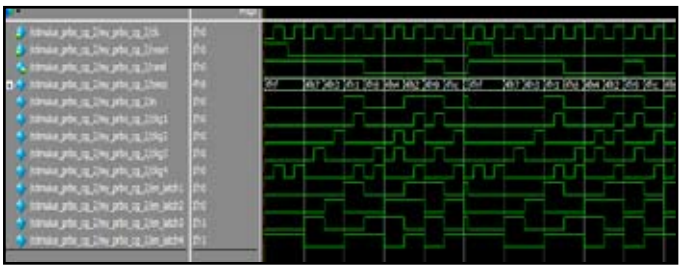

Fig. 8 : 4-bit Pseudo Random Binary Sequence generator (latch based design)

(iii). Flip-Flop Based Design

A fip-flop based design is exactly similar to the latch based design just the difference lies in the element controlling the state of enable signal , instead of a level sensitive latch, an edge triggered flip flop is involved in controlling the enable signal applied to the gate [1].

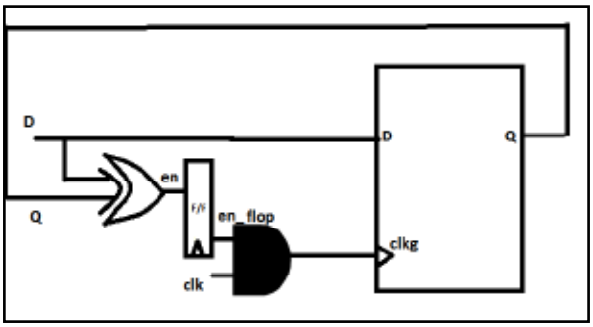

Fig. 9 : Negative edge triggered D flip flop (flip flop based design)

- These kinds of flip-flop based design are area and power-consuming.
- But advantage compared with gated-clock-based design is that testability can be easily implemented and clock skew is more manageable.

The simulation result of this type of clock gating technique on a D flip flop is as shown next in fig.10;

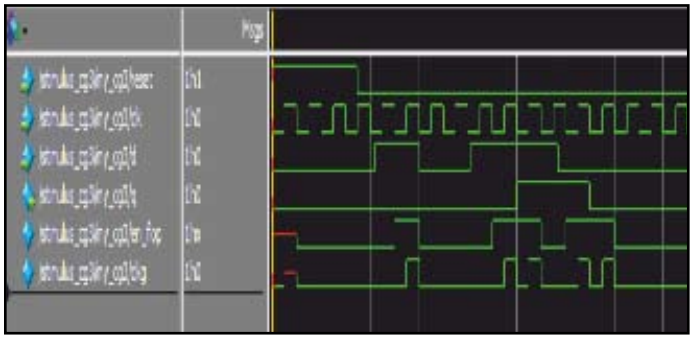

Fig. 10 : Negative edge triggered D flip flop (flip flop based design)

For the 4-Bit Pseudo Random Binary Sequence Generator the simulation results are as shown in fig.10.

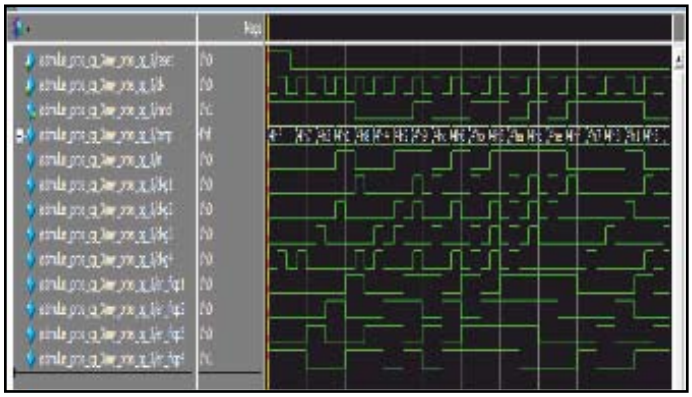

Fig. 11 : 4-Bit Pseudo Random Binary Sequence Generator (flip flop based design)

(iv). Intelligent clock gating

Intelligent clock gating is a set of algorithms that can detect unnecessary switching in the design and suppress it. This fully automated method adds a small amount of logic to suppress and minimize nonessential activity in the design, which reduces the power consumed by the design. Recently, in many industry sign-off tools like Cadence SOC Encounter, Altera, Xilinx etc intelligent clock gating option has been made available in the tool to optimize the power consumption of the design [1]. It is important to note that in such cases it may be possible that designer may not always get power reduction to desired level. Hence in such conditions designer may have to incorporate possible clock gating methods discussed above at RTL level to further reduce the dynamic power consumption of the circuit.

IV. Results & Conclusion

This paper presents a complete review of Clock Gating; one of the powerful power optimization techniques for VLSI circuit .The various advantages and disadvantages associated with each of these techniques is listed in table I. And to prove that this clock gating logic doesn't affect the functionality of a circuit, the simulation results too have been shown in table II.

Table 1: Comparison among Techniques

Technique	Advantage	Disadvantage
Latch-free	simple	glitches
Latch-based	Glitch-free	Not testable
Flip-flop	Testable	Power consuming

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Table 2 : Power Results With & Without CG

CIRCUIT	CLOCK Time period	DYNAMIC POWER(W)	TOTAL POWER (W)
D flip flop (no CG)	10 ns 1 ns 0.1ns 10 ps 1 ps	0.006 0.019 0.145 1.409 14.048	0.165 0.178 0.305 1.576 14.299
D flip flop (with CG)	10 ns 1 ns 0.1ns 10 ps 1 ps	0.006 0.019 0.144 1.399 13.951	0.165 0.178 0.304 1.566 14.202
PRBS (no CG)	10 ns 1 ns 0.1ns 10 ps 1 ps	0.006 0.019 0.141 1.370 13.660	0.165 0.178 0.301 1.537 13.911
PRBS (with CG)	10 ns 1 ns 0.1ns 10 ps 1 ps	0.006 0.018 0.129 1.12 12.500	0.165 0.177 0.290 1.287 12.511

Power optimization, traditionally relegated to the synthesis, and placement and routing stages, has moved up to the System level and RTL stages. Hardware designers can hence use clock gating to turn off inactive sections of the design and reduce overall dynamic power consumption.

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