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Efficient Test Pattern Generator for BIST using Multiple Single Input Change Vectors

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Abstract
Digital circuit's complexity and density are increasing while, at the same time, more quality and reliability are required. These trends, together with high test cost, make the validation of VLSI circuits more and more difficult. This paper proposes a novel test pattern generator (TPG) for built-in self-test. Our method generates multiple single input change (MSIC) vectors in a pattern, i.e., each vector applied to a scan chain is an SIC vector. According to the different scenarios of scan length, this paper develops two kinds of SIC generators to generate Johnson vectors and Johnson codeword's, i.e., the reconfigurable Johnson counter and the scalable SIC counter. The proposed TPG is flexible to both the test-per-clock and the test-per-scan schemes. A theory is also developed to represent and analyze the sequences and to extract a class of MSIC sequences. Analysis results have the favourable features of minimum transition of sequence, uniform distribution of pattern, uniqueness of pattern, and low hardware overhead.

Keywords
BIST, SIC, TPG, MSIC, CUT.

I. Introduction

A built-in self-test (BIST) is a mechanism that permits a machine to test itself. BIST techniques can effectively reduce the difficulty and complexity of VLSI testing, by introducing on-chip test hardware into the circuit-under-test (CUT). In conventional BIST architectures, the linear feedback shift register (LFSR) is commonly used in the test pattern generators (TPGs) and output response analyzers. A major drawback of these architectures is that the pseudorandom patterns generated by the LFSR lead to significantly high switching activities in the CUT [1], which can cause excessive power dissipation. They can also damage the circuit and reduce product yield and lifetime [2], [3]. In addition, the LFSR usually needs to generate very long pseudorandom sequences in order to achieve the target fault coverage in nanometer technology.

A. Existing method

Many advanced BIST techniques have been studied and applied. The first class is the LFSR tuning. Girard analyzed the impact of an LFSR's polynomial and seed selection on the CUT's switching activity, and proposed a method to select the LFSR seed for energy reduction [4].

The second class is low-power TPGs. One approach is to design low-transition TPGs. Wang and Gupta used two LFSRs of different speeds to control those inputs that have elevated transition densities [5]. Corno provided a low- power TPG based on the cellular automata to reduce the test power in combinational circuits [6]. Another approach focuses on modifying LFSRs. The scheme in [7] reduces the power in the CUT in general and clock tree in particular. In [8], a low-power BIST for data path architecture is proposed, which is circuit dependent. Bonhomme . [9] used a clock gating technique where two nonoverlapping clocks control the odd and even scan cells of the scan chain so that the shift power dissipation is reduced by a factor of two. The ring generator [10] can generate a single-input change (SIC) sequence which can effectively reduce test power. The third approach aims to reduce the dynamic power dissipation during scan shift through gating of the outputs of a portion of the scan cells. Bhunia [11] inserted blocking logic into the stimulus path of the scan flip-flops to prevent the propagation of the scan ripple effect to logic gates. The need for transistors insertion, however, makes it difficult to use with standard cell libraries that do not have power-gated cells. In [12], the efficient selection of the most suitable subset of scan cells for gating along with their gating values is studied.

The third class makes use of the prevention of pseudorandom patterns that do not have new fault detecting abilities [13],[14]. In [15], a pseudorandom BIST scheme was proposed to reduce switching activities in scan chains.

Other approaches include LT-LFSR [16], a low-transition random TPG [17]. The TPG in [16] can reduce the transitions in the scan inputs by assigning the same value to most neighboring bits in the scan chain. In [17], power reduction is achieved by increasing the correlation between consecutive test patterns.

II. Proposed Method

This section develops a TPG scheme that can convert an SIC vector to unique low transition vectors for multiple scan chains. First, the SIC vector is decompressed to its multiple code words. Meanwhile, the generated code words will bit-XOR with a same seed vector in turn. Hence, a test pattern with similar test vectors will be applied to all scan chains. The proposed MSIC-TPG consists of an SIC generator, a seed generator, an XOR gate network, and a clock and control block. According to the different scenarios of scan length, this paper develops two kinds of SIC generators to generate Johnson vectors and Johnson code words, i.e., the reconfigurable Johnson counter.

A. Test Pattern generation method

There are m primary inputs (PIs) and M scan chains in a full scan design, and each scan chain has l scan cells. The vector generated by an m-bit LFSR with the primitive polynomial can be expressed as $S(t) = S0(t)S1(t)S2(t), \ldots, Sm-1(t)$

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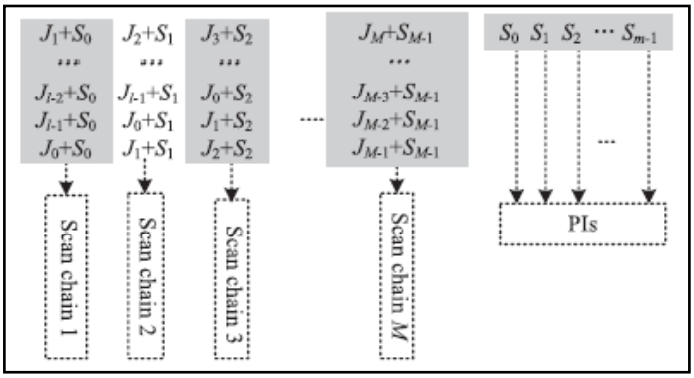

Fig.1 : Symbolic representation of MSIC pattern

(hereinafter referred to as the seed), and the vector generated by an l-bit Johnson counter can be expressed as J (t) = J0(t)J1(t)J2(t), . . . , Jl−1(t).The first clock cycle, J = J0 J1 J2, . . . , Jl−1 will bit-XOR with S = S0S1S2, . . . , SM−1, and the results X1Xl+1X2l+1, . . . , X(M−1)l+1 will be shifted into M scan chains, respectively. In the second clock cycle, J = J0J1 J2, . . . , Jl−1 will be circularly shifted as J = Jl−1 J0 J1, . . . , Jl−2, which will also bit-XOR with the seed S= S0S1S2, . . . , SM−1. The resulting X2Xl+2X2l+2, . . . , X(M−1)l+2 will be shifted into M scan chains, respectively. After l clocks, each scan chain will be fully loaded with a unique Johnson codeword, and seed S0S1S2, . . . , Sm−1 will be applied to m PIs. Therefore circular Johnson counter can generate l unique Johnson code words through circular shifting a Johnson vector, the circular John son counter and XOR gates in Fig. 1 actually constitute a linear sequential de compressor.

B. Reconfigurable Johnson Counter

For a short scan length, we develop a reconfigurable Johnson counter to generate an SIC sequence in time domain. As shown in Fig.2, it can operate in three modes.

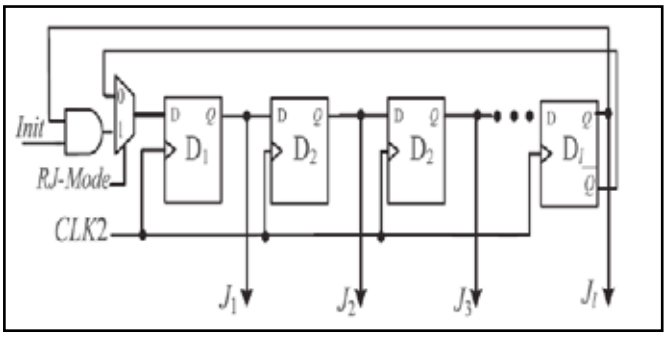

Fig. 2 : Reconfigurable Johnson counter

1) Initialization: When RJ_Mode is set to 1 and Init is set to logic 0, the reconfigurable Johnson counter will be initialized to all zero states by clocking CLK2 more than l times.
2) Circular shift register mode: When RJ_Mode and Init are set to logic 1, each stage of the Johnson counter will output a Johnson codeword by clocking CLK2 l times.
3) Normal mode: When RJ_Mode is set to logic 0, the reconfigurable Johnson counter will generate 2l unique SIC vectors by clocking CLK2 2l times.

C. Scalable SIC counter

When the maximal scan chain length l is much larger than the scan chain number M , we develop an SIC counter named the "scalable SIC counter."

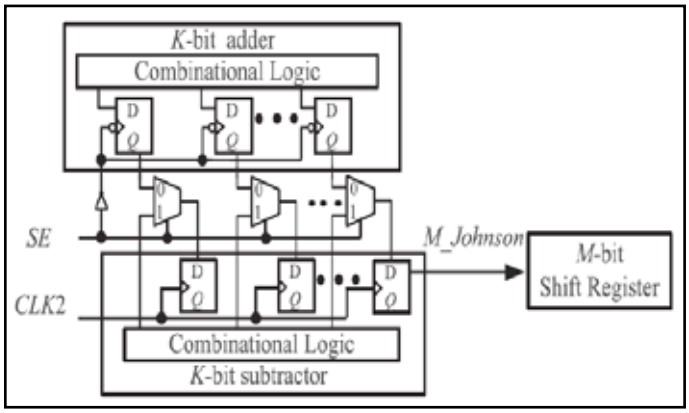

Fig. 3 : Scalable SIC counter

As shown in Fig. 3, it contains a k-bit adder clocked by the rising SE signal, a k-bit subtractor clocked by test clock CLK2, an M -bit shift register clocked by test clock CLK2, and k multiplexers. The value of k is the integer of log2(l-M). The k-bit adder is clocked by the falling SE signal, and generates a new count that is the number of 1s (0s) to fill into the shift register. As shown in Fig. 3, it can operate in two modes.

1. If SE = 1 and the contents of the k-bit subtractor are not all zeros, M-Johnson will be kept at logic 1 (0).
2. Otherwise, it will be kept at logic0 (1). Thus the needed 1's (0s) will be shifted into the M-bit shift register by clocking CLK2 l times, and unique Johnson code words will be applied into different scan chains.

D. Scan Chains

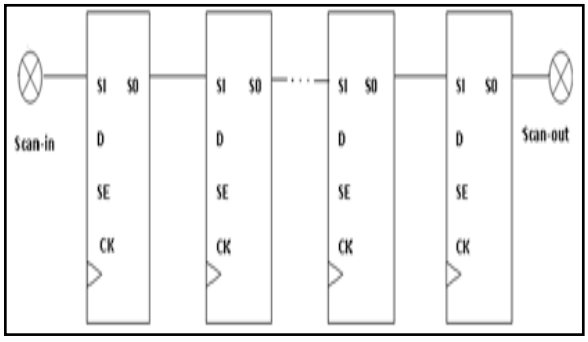

Fig. 4 : Scan Chain

Scan chains are the elements in scan-based designs that are used to shift-in and shift-out test data. A scan chain fig (4) is formed by a number of flip flops connected back to back in a chain with the output of one flip flop connected to another. The input of first flip flop is connected to the input pin of the chip(called scan-in) from where scan data is fed. The output of the last flip flop is connected to the output pin of the chip called (scan-out) which is used to take the shifted data out.

E. MISR

In test-per-scan scheme, the testing phase of the TPG fils the scan chains which will apply their contents to the circuit under test(CUT). All the scan outputs are connected to the multiple input signature register (MISR), which will perform signature compaction. The possibilities to speedup the test process by using multiple scan chains or by using a partial scan solution. It is shown in fig (5).

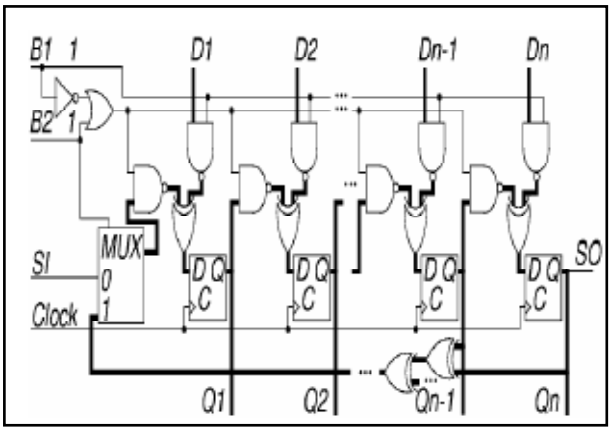

Fig. 5 : MISR

III. Msic Sequences

The proposed algorithm is to reduce the switching activity. In order to reduce the hardware overhead, the linear relations are selected with consecutive vectors or within a pattern, which can generate a sequence with a sequential de compressor, facilitating hardware implementation. Another requirement is that the MSIC sequence should not contain any repeated test patterns, because repeated patterns could prolong the test time and reduce test efficiency. Finally, uniformly distributed patterns are desired to reduce the test length i.e., number of patterns required to achieve a target fault coverage

A. MSIC-TPGs for Test-per-Clock Schemes

The MSIC-TPG for test-per-clock schemes is illustrated in Fig. 6. The CUT's PIs $X_1 - X_{mn}$ are arranged as an $n \times m$ SRAM-like grid structure. Each grid has a two-input XOR gate whose inputs are tapped from a seed output and an output of the Johnson counter. The outputs of the XOR gates are applied to the CUT's PIs. A seed generator is an m-stage conventional LFSR, and operates at low frequency CLK1. The test procedure is as follows.

1. The seed generator generates a new seed by clocking CLK1 one time.
2. The Johnson counter generates a new vector by clocking CLK2 one time.
3. Repeat 2 until 2l Johnson vectors are generated.
4. Repeat 1–3 until the expected fault coverage or test length is achieved.

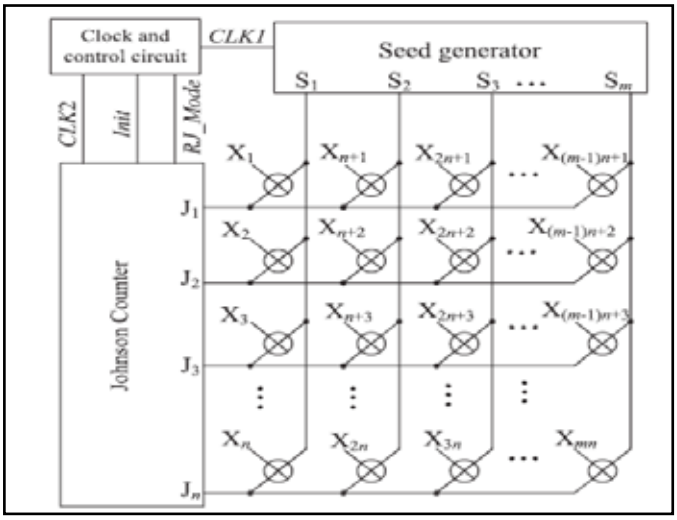

Fig. 6 : Test-Per-Clock

B. MSIC-TPG for Test-per-scan schemes

The MSIC-TPG for test-per-scan schemes is illustrated in Fig. 7. The stage of the SIC generator is the same as the maximum scan length, and the width of a seed generator is not smaller than the scan chain number. The inputs of the XOR gates come from the seed generator and the SIC counter, and their outputs are applied to M scan chains, respectively. The output of the seed generator and XOR gates are applied to the CUT's PIs, respectively. The test procedure is as follows.

1. The seed circuit generates a new seed by clocking CLK1 one time.
2. RJ_Mode is set to "0". The reconfigurable Johnson counter will operate in the Johnson counter mode and
3. generate a Johnson vector by clocking CLK2 one time.
4. After a new Johnson vector is generated, RJ_Mode and Init are set to 1. The reconfigurable Johnson counter operates as a circular shift register, and generates l codewords by clocking CLK2 l times. Then, a capture operation is inserted.
5. Repeat 2–3 until 2l Johnson vectors are generated.
6. Repeat 1–4 until the expected fault coverage or test length is achieved.

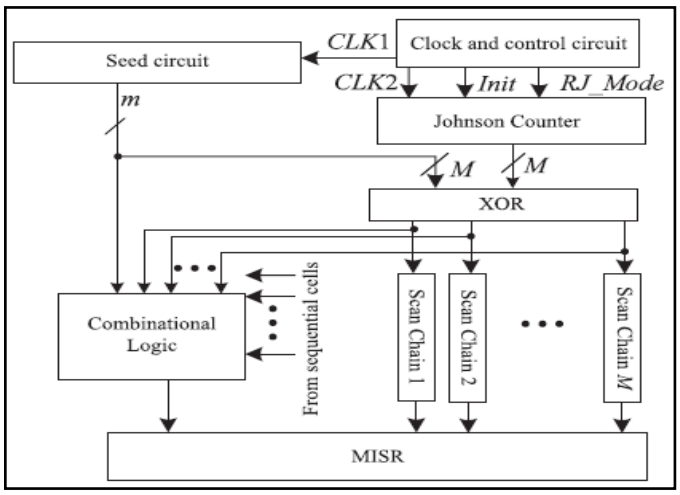

Fig .7 : Test -Per-Scan scheme

III. Simulation Results

The proposed architecture is designed using verilog HDL, simulated using modelsim software and synthesized using Xilinx project navigator. The simulated output for the proposed MSIC test pattern generator shown below.

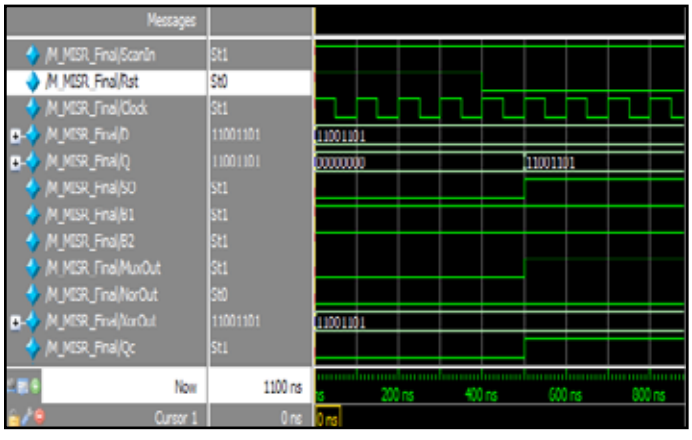

Fig. 8 : MISR

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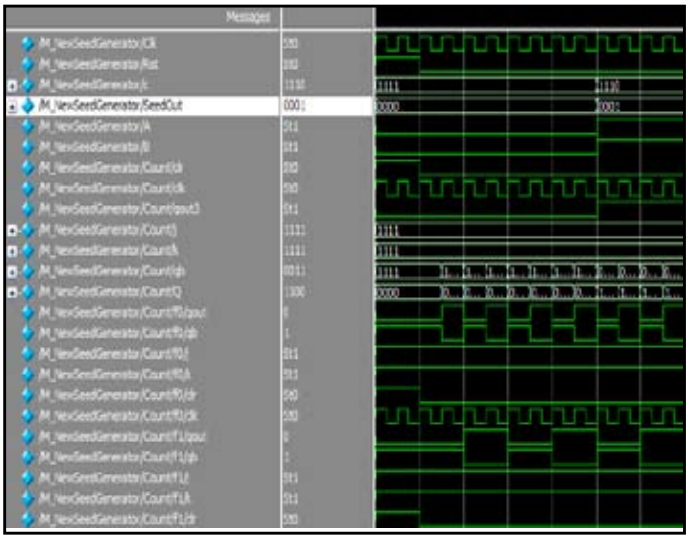

Fig. 9 : Seed Generator

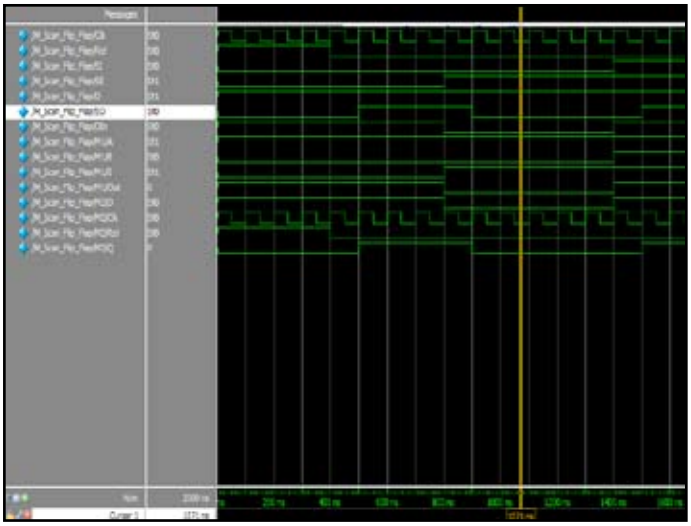

Fig. 10 : Scan flipflop

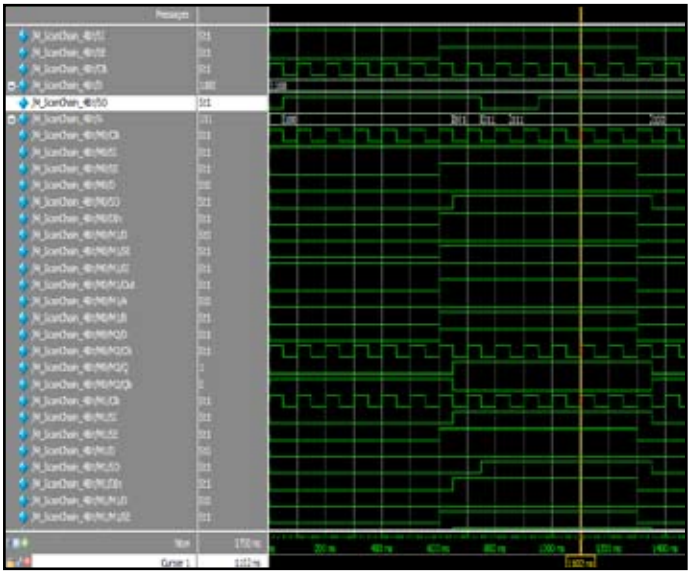

Fig .11 : Scan chain

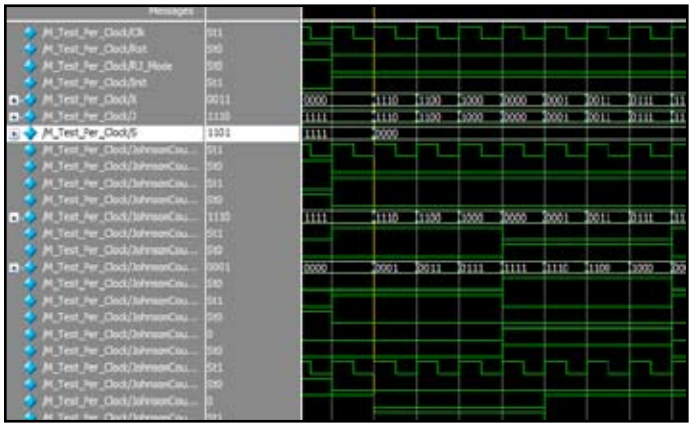

Fig.12 : Test per clock (Johnson counter based)

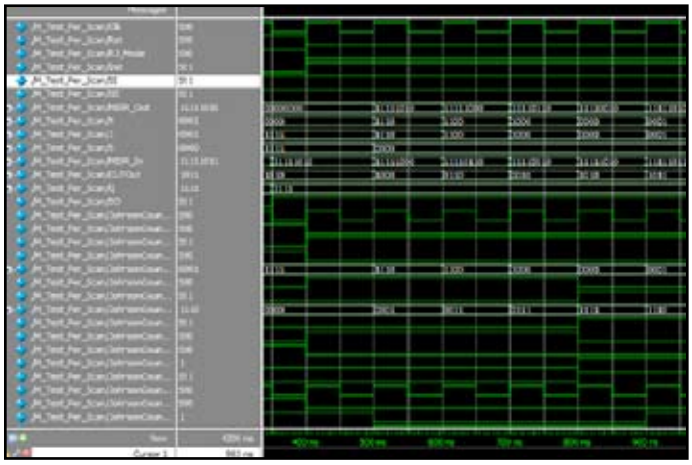

Fig.13 : Test per scan (Johnson counter based)

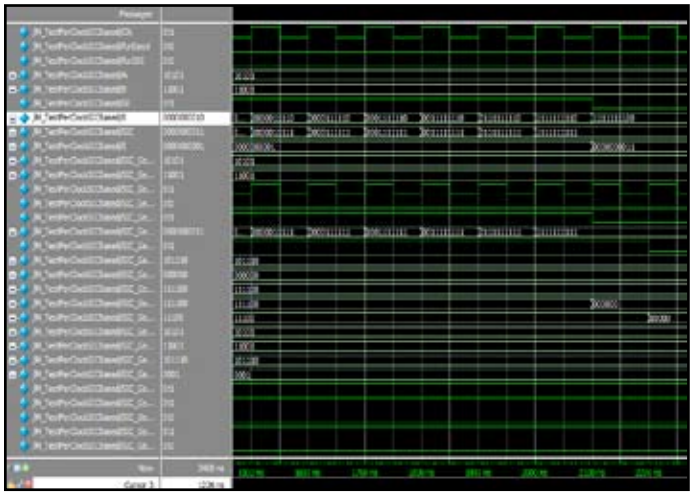

Fig.14 : Test per clock (SIC counter based)

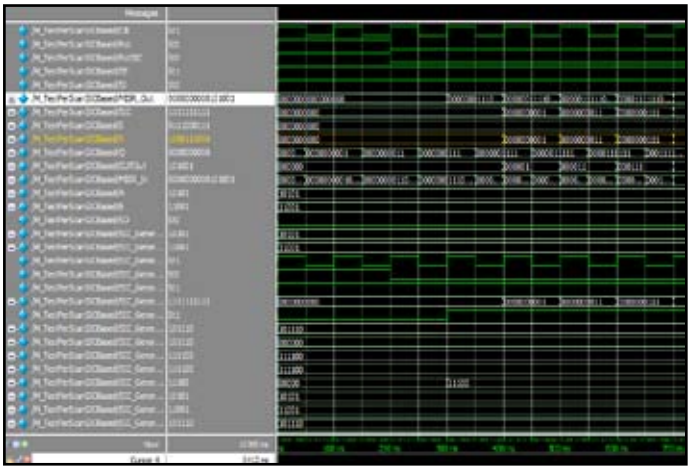

Fig.15 : Test per scan (SIC counter based)

V. Comparison

Experiments on ISCAS'85 benchmarks and standard full-scan designs of ISCAS'89 benchmarks are conducted to analyze the performance of the proposed MSIC-TPG. The performance simulations are carried out with the Synopsys Design Analyzer and Prime Power . The area overheads of MSIC and LFSR are 21%–157% and 22%–258% respectively. The MSIC-TPG thus incurs less area overhead than the LFSR. The number of total equivalent gates is about 2309 for the conventional LFSR and 1089 for the MSIC-TPG. The MSIC-TPG saves 25%–50.0% total power and 15.6%–32.6% peak power against the conventional LFSR.

VI. Conclusion

This paper has proposed a low-power test pattern generation method that could be easily implemented by hardware. It also developed a theory to express a sequence generated by linear sequential architectures, and extracted a class of SIC sequences named MSIC. Analysis results showed that an MSIC sequence had the favorable features of uniform distribution, low input transition density, and low dependency relationship between the test length and the TPG's initial states. Combined with the proposed reconfigurable Johnson counter or scalable SIC counter, the MSIC-TPG can be easily implemented, and is flexible to test-per-clock schemes and test-per-scan schemes. For a test-per-clock scheme, the MSIC-TPG applies SIC sequences to the CUT with the SRAM-like grid. For a test-per- scan scheme, the MSIC-TPG converts an SIC vector to low transition vectors for all scan chains. Experimental results and analysis results demonstrate that the MSIC-TPG is scalable to scan length, and has negligible impact on the test overhead. After the generating the MSIC, in this we conduct the validation process on the combinational logic circuit and verified the output.

V. Acknowledgement

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