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A Topology for 9-Level Multilevel Inverter with Converting Its Optimal Structure

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Abstract
Multilevel Inverter is a such type of inverter which has a ability of functioning in high power , high voltage with reduced total harmonic distortion, less switching losses ,better power quality than conventional inverter with increase the voltage level and working on high power ,high voltage application ,They have become more popular. There are some drawbacks also in multilevel inverter that their difficulty and requires large number of power devices and requires composite controllability. This paper presents a noble multilevel inverter topology using one bidirectional switch and other unidirectional switches which is used in single phase 9-level multilevel inverter.. By this topology, number of power switches can be minimized with minimum complexity as compare to other conventional multilevel inverter methods

Keywords
Multi-level inverter (MLIs); OPTIMIZATION and different PWM techniques.

I. Introduction

Multilevel concept started with 3- level converter. Then, quite a few multilevel converter topologies have been urbanized. However, the simple concept of a multilevel converter to attain higher power is to use a series of power semiconductor switches with several lower voltage dc sources to execute the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and renewable energy voltage sources can be worked as the multiple dc voltage sources. Though, the rated voltage of the power semiconductor switches depends only upon the rating of the dc voltage sources to which they are linked. The main area of multilevel inverter has traction, both in locomotives and track-side static converters. A multilevel inverter enhance the quality of output MLI have received more and more consideration because of efficiency and low electromagnetic interference(EMI) [5].The three types of multilevel converter structures explained in the literature are cascaded H-bridge converter with separate dc sources, diode clamped (neutral-clamped), and flying capacitors (capacitor clamped)[1]. Modulation techniques and control have been urbanized for multilevel converters such as Sinusoidal pulse width modulation (SPWM), selective harmonic elimination (SHE-PWM), space vector modulation (SVM), and others. Many, multilevel converter applications comprise industrial medium-voltage motor drives, renewable energy systems with utility interface, flexible AC transmission system (FACTS), and traction drive systems.[4] The frequent multilevel converter topologies are the neutral-point-clamped converter (NPC), flying capacitor converter (FC) and Cascade H-Bridge (CHB) have urbanized from last two decades. Multilevel inverters are most excellent for medium and high power applications.

The control method of cascaded H Bridge multilevel is more convenient than other multilevel inverter because it have no any clamping diode and flying capacitor. Cascaded multilevel inverter reaches higher consistency. The cascaded inverter is used for bulky automotive electric drives .However, the necessity of more number of switches and separate dc source for each cell becomes a problem particularly at higher level [9-11]. This paper presents a 7-level multi-level inverter which requires reduce number of switches and gate driver circuits as compared to predictable multilevel inverters. Now there is implemented in single-phase different PWM techniques. The pulse-width modulation (PWM) control is the most well-organized method of controlling output voltage within the inverters. The carrier based PWM schemes used for multilevel inverters is the mainly capable method, realized by the intersection of a modulating signal with triangular carrier waveform. The paper tries to verify that optimization method is superior than conventional multilevel inverters in terms of their number of components and THD.

II. Proposed Topology

The circuit diagram of multi-level inverter using optimization topology is shown in Fig. 2.1. In this figure, the right side h-bridge is connected which is used to generates positive and negative level.

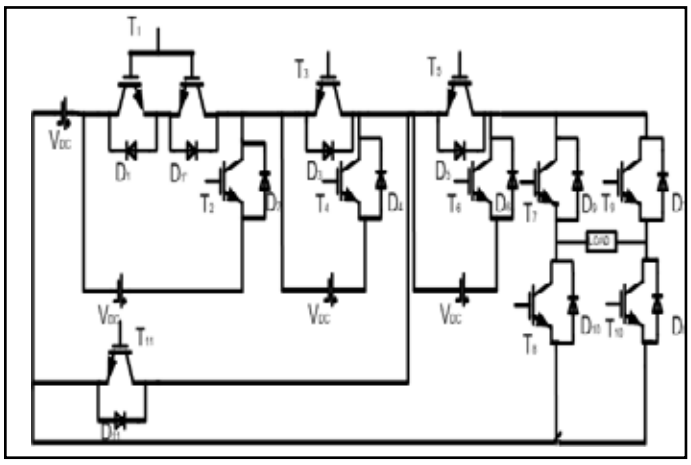

Fig.2: single phase 9-Level Multilevel Inverter with Converting Its Optimal Structure

The main purpose of this paper is to manage the EMI, diminish the total harmonic distortion with different PWM techniques using Optimization topology and it also minimize power semiconductor switches than conventional multilevel inverter. For a conventional single-phase 9-level inverter model, it uses 16 switches, whereas the proposed model uses only 11 switches in which one switch is bidirectional[12]. This optimization multilevel inverter easily extends to higher voltage levels by growing the middle section as shown in Fig. 2.1 fixed dc voltage values. In evaluation with a cascade topology, it requires just one-third of inaccessible power

supplies used in a cascade-type inverter. The operation of the anticipated topology has been discussed in element and has been confirmed with the help of simulations. The planned topology is a symmetrical topology since all the values of all voltage sources are same.

This MLI topology has been proposed which reduces the overall number of switching devices from conventional MLI topology. They has less count of power devices as compare to cascaded h-bridge MLI as shown in Fig.1. It has three separate dc source as 7-level MLI. The new proposed topology can be easily extended to any required number of voltage levels by increasing the middle part of circuit. This proposed topology is same topology with all voltage sources have equal value and similar to be used for single-phase MLI. The proposed 9-level MLI can operates in different modes which are as given. Operation of the single-phase 9-level MLI with new optimization can be easily explained with the help of fig. 2 and table. When switches T1, T3, T5 , T7 and T10 are turned "on" the output voltage will be "Vdc" (level 1). The output voltage will be "2Vdc" (i.e., level 2) when switches T2,T3, T6, T7 and T10 are turned "on". When T2, T4, T5, T7 and T10 switches are turned "on" the output voltage will be "3Vdc" (i.e., level 3). When T2, T4, T6, T7 and T10 switches are turned "on" the output voltage will be "4Vdc" (i.e., level 4). When switches T6,T5, T7 and T10 are turned "on" the output voltage is zero (i.e., level 0). Switches T9, T8, T7 and T10 are used for a opposite pair. When T7 and T10 are turned "on" mutually, positive half cycle (level +1, level +2, level +3,level +4) can be generated and when T8 and T9 are turned "on" together, negative half cycle (level -1, level -2, level -3,level -4) .The operation of this topology can also be easily implicit by mode of operation of single-phase 9-level MLI shown in figure 2. Each voltage source "Vdc" is required 100V. There are nine sufficient switching modes in generating the multistep level for a 9-level MLI.

Table 1 : Switching mode 9-level MLI

VOLTAGE LEVEL	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	OUTPUT VOLTAGE
4	0	1	0	1	0	1	1	0	0	1	0	4Vdc
3	1	0	1	0	1	0	1	0	0	1	0	3Vdc
2	0	1	1	0	0	1	1	0	0	1	0	2Vdc
1	0	1	1	0	0	1	1	0	0	1	0	Vdc
0	0	0	0	0	1	1	1	0	0	1	1	0
-1	0	1	1	0	0	1	0	1	1	1	0	-Vdc
-2	0	1	1	0	0	1	0	1	1	0	0	-2Vdc
-3	1	0	1	0	1	0	0	1	1	0	0	-3Vdc
-4	0	1	0	1	0	1	0	1	1	0	0	-4Vdc

III. Modulation Strategies

There are different pulse width modulation strategies with different phase relationships.

Phase disposition pulse width modulation (PD PWM)

In phase disposition pulse width modulation strategy, where all carrier waveforms are in same phase shown in fig 3.1 for 5-level MLI For 7-level MLI, 6 triangle carriers are required. For 9-level MLI, 8- triangle carriers are required [1-5].

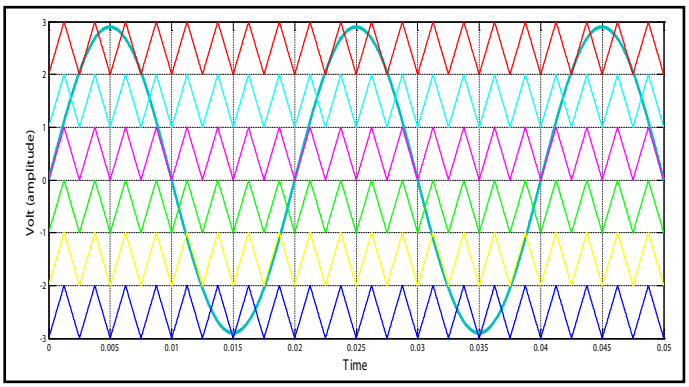

Fig. 3.1: Carrier arrangement for PDPWM strategy (ma=0.9 and mf=20)

Phase opposition disposition pulse width modulation (POD PWM)

In phase opposition disposition pulse width modulation strategy, where all carrier waveforms above zero reference are in phase and below zero reference are opposite of phase. Shown in fig 3.2[9-11].

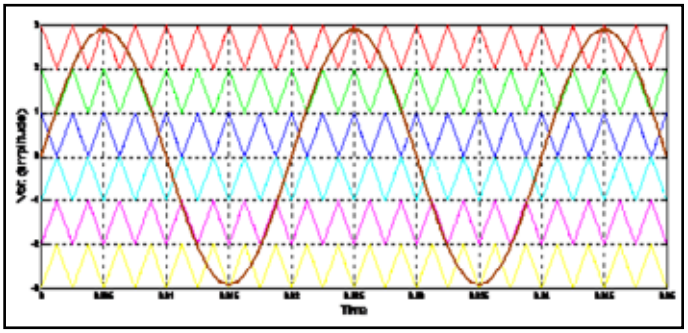

Fig. 3.2: Carrier arrangement for PODPWM strategy (ma=0.9 and mf=20)

Alternate phase opposition disposition pulse width modulation (APOD PWM)

In alternate phase opposition disposition PWM scheme where every carrier waveform is in out of phase with its neighbor carrier oppositely shown in fig 3.3[9-11].

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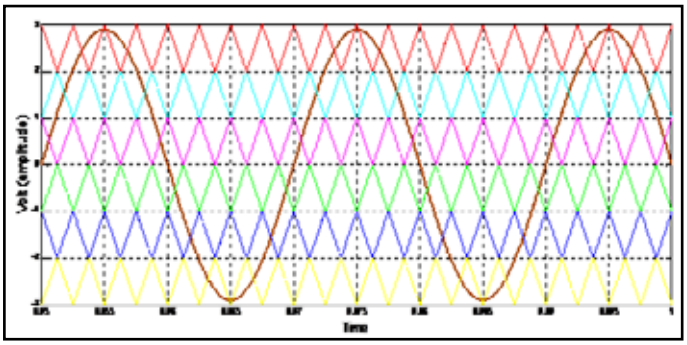

Fig. 3.3: Carrier arrangement for APODP strategy (ma=0.9 and mf=20)

Phase-shifted pulse width modulation (PS PWM)

Fig.3.4 shows the carrier Phase-shifted pulse width modulation strategy. A carrier phase shifted PWM for multi-level inverter is used to produce the stepped multi-level output voltage waveform with lower % THD. In phase shifted PWM, all the triangular carriers have similar frequency and same peak to peak amplitude [9-11].

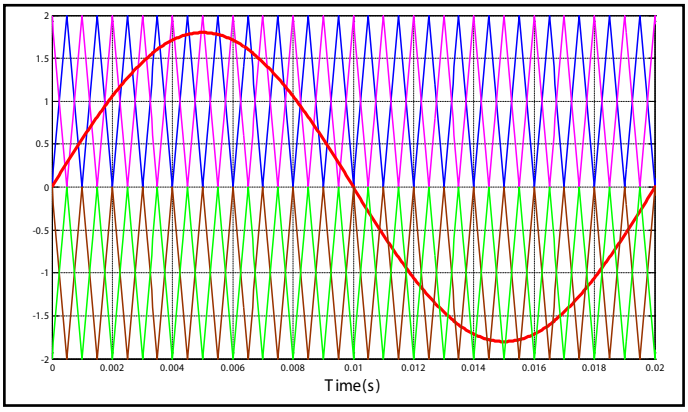

Fig. 3.4: Carrier arrangement for PSPWM strategy (ma=0.9 and mf=20

Inverted Sine Phase carrier pulse width modulation (ISPOD PWM)

In inverted sine phase opposition techniques inverted sine pulse are at 0 degree at below zero and above zero it is 180 degree out of phase.

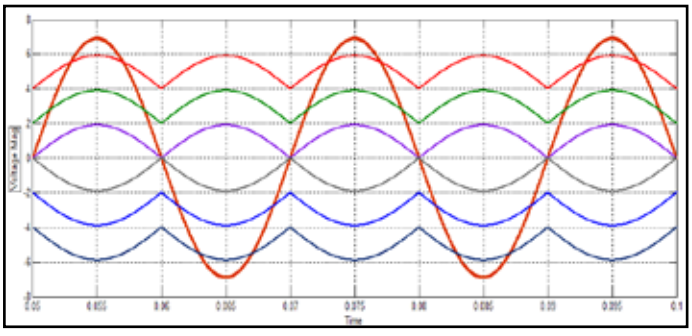

Fig. 3.4: Carrier arrangement for ISCPWM strategy (ma=0.9 and mf=20

Variable frequency pulse width modulation (VFPOD PWM)

In variable frequency techniques inverted sine pulse , there are 6 pulse which is different variable frequency are compared with sine pulse.

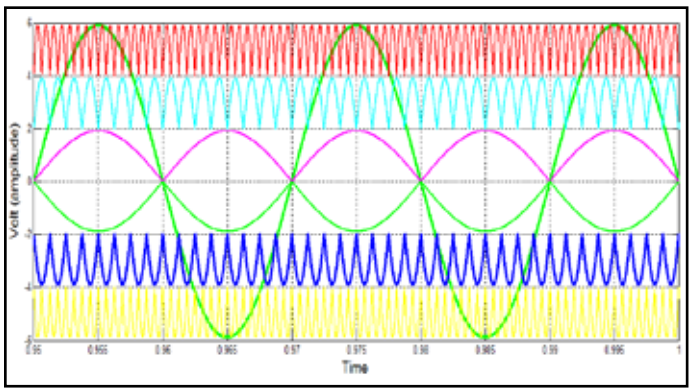

Fig. 3.4: Carrier arrangement for VFPWM strategy (ma=0.9 and mf=20

IV. Output Waveform

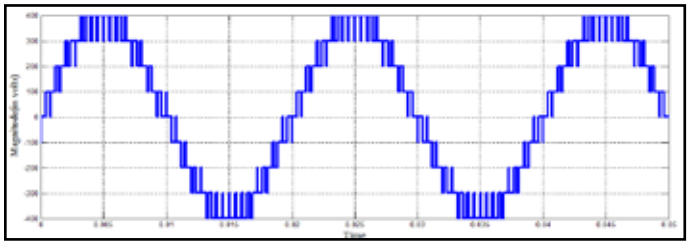

Fig. 5:Output voltage waveform of 9-Level Multilevel Inverter with converting Its Optimal Structure

V. Simulation Results

The Fig. 2.1 & 2.2 shows the OT model of single-phase & three-phase 9-level RV MLI. Table II shows THD comparison between different PWM techniques. The simulation parameters are as following : dc source voltage is 100V; Frequency of carrier signal is 1 kHz. In this paper, four PWM techniques are used PD, POD, APOD, and PS with different modulation index (Ma). For Ma = 0.9, and Mf = 20, corresponding (%) THD are PD=14.66,POD =14.49,APOD=14.45,PS=14.49,ISC=14.52,VF-=15.09 shown in Fig. 4a – 4.f. Based on the PWM techniques, the harmonic spectrum was analysed by the FFT harmonic spectrum using the FFT Window in MATLAB/Simulink.

1. FFT Analysis

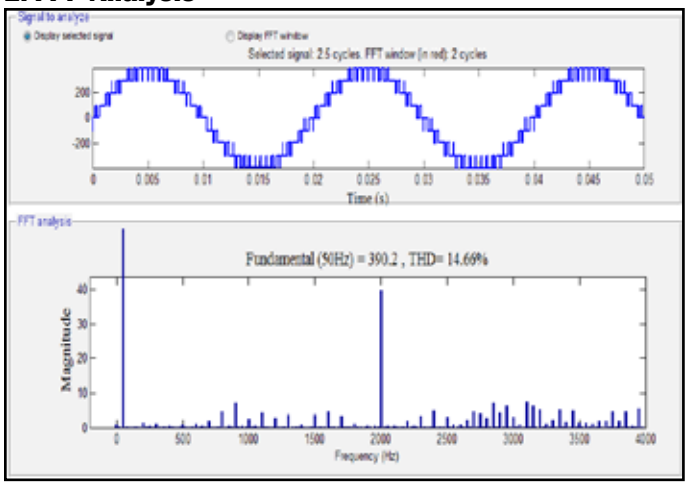

Fig. a: FFT analysis by PDPWM for R-L load (Ma=0.9, Mf=40)

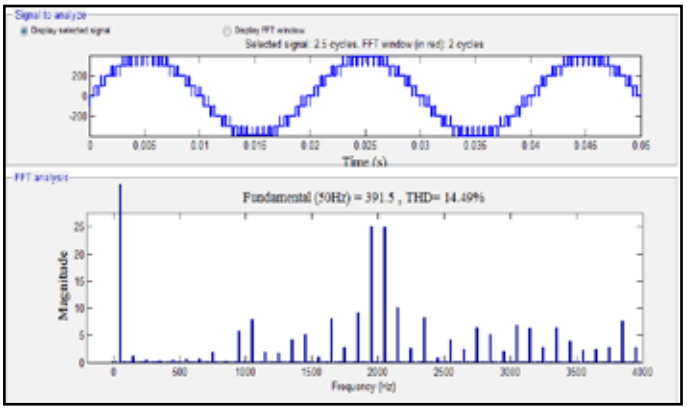

Fig. b: FFT analysis by PODPWM for R- load (Ma=0.9, Mf=40).

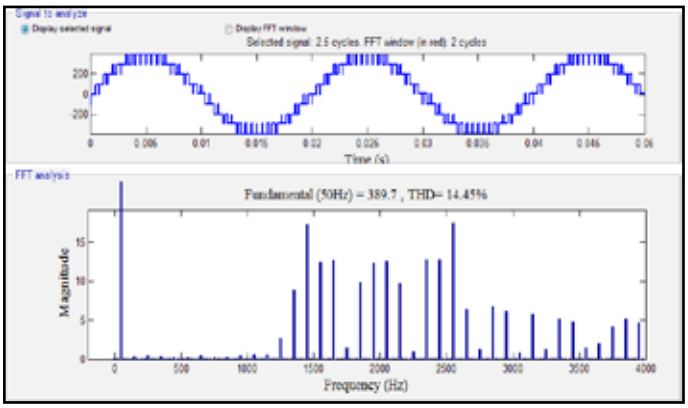

Fig. c: FFT analysis by APODPWM for R- load (Ma=0.9,Mf=40)

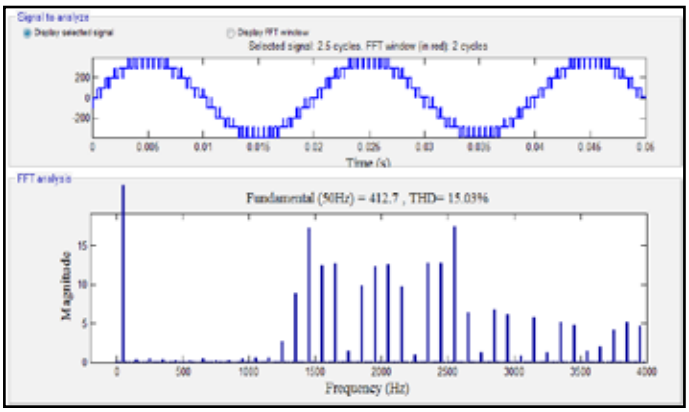

Fig. d: FFT analysis by PSPWM for R- load (Ma=0.9,Mf=40)

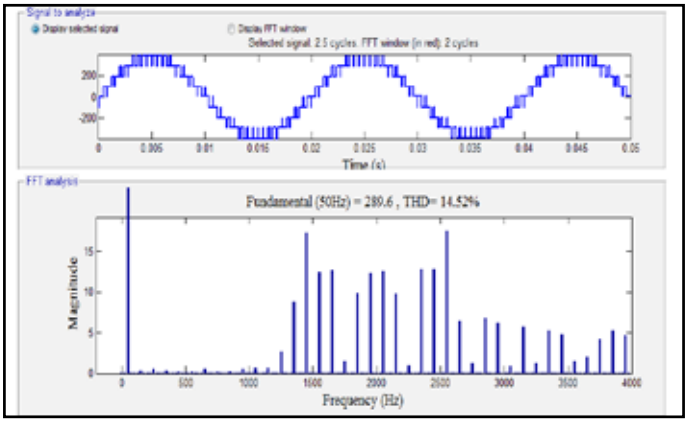

Fig. e: FFT analysis by ISCPWM for R- load (Ma=0.9,Mf=40)

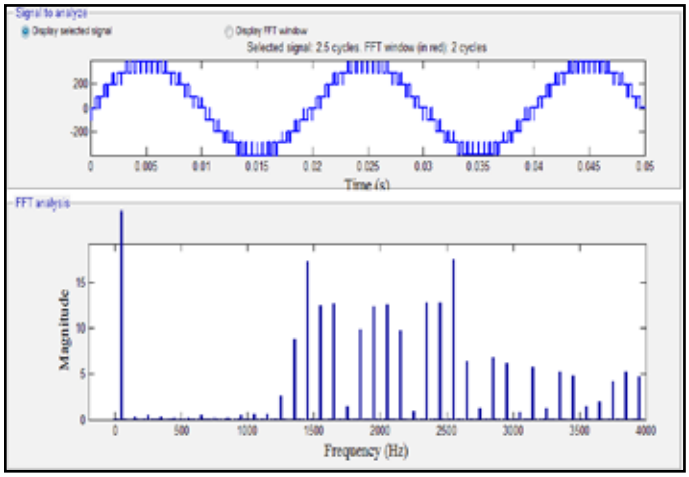

Fig.f: FFT analysis by VFPWM for R- load (Ma=0.9,Mf=40

(a) Phase disposition pulse width modulation (PD)
(b) Phase opposition disposition pulse width modulation (POD)
(c) Alternate phase opposition disposition pulse width modulation (APOD)
(d) Phase shift pulse width modulation (PSPOD)
(e) Inverted Sine Carrier pulse width modulation (ISCPOD)
(f) Variable Frequency pulse width modulation (VFPOD)

Table-2: Comparison between different multilevel inverter topologies

Modulation Index	PD %THD	POD %THD	APOD %THD	APOD %THD	APOD %THD	APOD %THD
0.933	21.36	21.10	20.93	20.93	20.93	20.93
0.966	20.04	19.740	19.746	19.746	19.746	19.746
0.990	18.672	18.44	18.54	18.54	18.54	18.54
1.000	18.24	18.14	18.36	18.36	18.36	18.36

Table 3: Comparison between different multilevel inverter topologies

Inverter Topologies	CHB	NPC	Flying capacitor	Proposed Topology
Power Switches	14	16	14	11
Main diode	0	0	0	0
Clamping Diode	0	32	0	0
DC bus Capacitor	0	7	7	0
Flying Capacitor	0	0	17	0
DC source	4	1	1	4

VI. Conclusion

In this paper, a 9-level multi-level inverter using optimal topology is proposed with different PWM techniques and it is used to generate 9-level output voltage. This topology has been explained with presented topology. It is proved that the proposed work of Single phase 9-level MLI output voltage total harmonics distortion is minimized and improve the efficiency of system compare with different conventional topologies of single phase 9-level MLI. Table-3 shows the number of power switches [IGBTs] and output voltage steps in the proposed topology. This proposed MLI

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topology requires less number of components as compared to conventional MLI inverters.

References

[1] *S. Daher, J. Schmid, and F. L. M. Antunes, "Multilevel inverter topologies for stand-alone PV systems, " IEEE Trans. Ind. Electron vol. 55, pp.2703-2708,Jul. 2008*

[2] *Hemant Joshi, P. N. Tekwani and Amar Hinduja Kolorrol "Multilevel Inverter For Induction Motor Drives Using RV Topology," Vol. 3A-28 IEEE Trans. Ind. 2010.*

[3] *K. Jang-Hwan, S.-K. Sul, and P. N. Enjeti, "A carrier-based PWM method with optimal switching sequence for a multilevel four-leg voltage source inverter," IEEE Trans. Ind. Applc., vol. 44,pp. 1239–1247, Jul./Aug. 2008.*

[4] *X.Yuan and I.Barbi, "Fundamentals of a New Diode Clamping Multilevel Inverters", IEEE Transaction Power Electron., Vol.15, No.4, 2000, pp.711-717.*

[5] *Jose Rodriguez, Jih-Sheng Lai and Fang Zheng Peng. "Multilevel Inverters: A survey of topologies, controls and applications." Ind.Electronics.vol-49 no.4 pp 724-737,Aug*

[6] *E. Babaei, "Optimal topologies for cascaded sub-multilevel converters, Power Electron., vol. 10, no. 3, pp. 251–260, May 2010.*

[7] *Nabe, I. Takahashi and H. Akagi. "A new neutral point clamped PWM inverter." IEEE Trans. Ind. Applicat. Vol. 1A-17, pp 518- 521, sep. /oct. 1981.*

[8] *E.Najafi, A.H.M.Yatim and A.S.Samosir. A new topology-reversing voltage (RV) for multi-level inverters." 2nd International pp 604-606,Decembe 2008Malaysia. conference*

[9] *E. Babaei," A casecaded MLI converter topology with rreduced number of switches",IEEE Transaction Power Electronics 23(6) (2008) 2657-2664.*

[10] *J.E.Brahimi,E Babaei,G.B.Gharchpehan ,"A new multilevel converter topology with reduced number of power electronics components" IEEE Transaction Power Electronics 59(2) (2012),655-663.*

[11] *J.Dixon,L.Moran, "High-level multistep inverter optimization using a minimum number of power transistor",IEEE Trans. Power Electronics 21(2)(2006),330-332*